

## AMENDMENTS TO THE SPECIFICATION

**Please delete the paragraph starting on page 4, line 23.**

**Please amend the paragraph starting on page 7, line 8 as follows:**

The designs of both identical consecutive digit circuit 102 and identical consecutive digit circuit 112 are described in more detail below with reference to ~~FIGs. 2-7~~FIGs. 2-6.

**Please amend the paragraph starting on page 11, line 11 as follows:**

Corresponding logic equations for each of the bits, B0-B3, of the binary code appear in ~~FIG. 7~~FIG. 6. Note that each of these logic equations can be implemented by using one or more OR gates. In the general case of an  $n$ -bit one-hot code, each bit of the binary code is associated with  $n/2$  bits of the one-hot code. Hence,  $n/2$  bits of the one-hot code are ORed together to produce each bit in the binary code. This can be accomplished using  $\lceil \log_2 n \rceil - 1$  levels of 2-input OR gates.